Presentation Abstracts

[Presentation 1] "Desensitization of an FM Receiver from an LCD Clock," by Shenhui Jing, Jun Fan
Abstract: A thorough characterization of an inter-system interference problem in a MP3 player device was performed to understand the coupling mechanism. The rising time effect of LCD clock line signal for noise coupling was identified from previous study. Noise source model for mounted IC and victim model for FM tuner were created and validated through measurement. Possible coupling paths were investigated by S21 measurements, and near field scanning was applied to identify noise sources. Two major coupling paths were identified. One is the LCD clock line going from CPU to LCD through the flex cable, and the other one is the audio lines connected to the headphone.

[Presentation 2] "Investigation of Interference in a Mobile Phone from a DC-to-DC Converter," by Satyajeet Shinde, David Pommerenke
Abstract: Turning ON the LCD screen of a cell phone causes desensitization of its receiver in one band. We present methods for the identification of sources, coupling mechanisms and coupling paths. Further possible suppression techniques are presented.

[Presentation 3] "EM Susceptibility of Medical Devices" by Ji Chen
Abstract: The heating of orthopedic implants under MRI RF fields were investigated 1.5T and 3T systems. Modeling and experiments were performed on an orthopedic device at different sizes inside an ASTM phantom. It is observed that the induced energy deposition near the device is almost linearly related to the dimension of the orthopedic implants when the device is less than 10 cm in length. Higher temperature rises were found in 1.5T for both computational and experimental studies.

[Presentation 4] "Highly Sensitive Electric and Magnetic Field Probes for RFI Near Field Scanning," by Guanghua Li, David Pommerenke
Abstract: Highly sensitive probes allow detecting weak field strengths for analyzing RFI problems, which cannot be measured by standard probes. The sensitivity of the system depends on probe size, Q-factor of the probe, thermal noise in the probe and amplifier. We investigate how to optimize the system sensitivity while keeping the spatial resolution as good as possible.

Abstract: The RF noise voltage received by an antenna due to near-field coupling is estimated using reciprocity, where the multiple scattering effect is neglected. This could be used for certain RF interference studies where the dominant noise mechanism is near-field coupling.

[Presentation 6] “Modeling of Roughness of PCB Traces,” by Ji Chen
Abstract: The analysis of conductor loss for a transmission line with arbitrary cross-section and periodic surface roughness along the propagation direction is presented in this paper. The frequency dependent skin-effect and proximity are both considered in the analysis. The per-unit-length impedance is extracted by assuming smooth metal surface. Modified surface impedance account for the periodic metal surface roughness is then incorporated for high-frequency correction.

The first step is to extract a series per-unit-length impedance as a function of frequency without considering the skin-depth and current crowding effect. The compact 2D-FDTD solver is used to model the entire cross-sectional geometry (possibly inhomogeneous) assuming metals are perfect electric conductor. To analyze the skin-depth as well as the current crowding effect, the obtained electromagnetic field distribution on the surface is then used as the boundary condition to analyze the current distribution inside the conductor; the conductor-only model is then built in the 2D-FDTD solver with finer meshes to capture the current redistribution as a result of finite conductivity. The equivalent surface impedance of the conductor is therefore obtained with a scale factor extracted as a function of the location on the circumference of the conductor. Upon the series per-unit-length impedance is solved, the fine features of the metal surface roughness is modeled as periodic protrusions. The active reflect coefficient is calculated to obtain the surface impedance for the rough metal, served as the normalized value in the scaled surface impedance function.

[Presentation 7] “PCB Conductor Surface Roughness as an Effective Dielectric Layer,” by Koledintseva Marina
Abstract: A simple model to substitute conductor surface roughness in printed circuit boards by a layer with an effective material lossy dielectric is proposed and tested using the 2D finite-element method (FEM) electromagnetics numerical simulations. The results of numerical modeling of a multilayered structure corresponding to a stripline transmission line with substituted roughness are compared with the experimental results obtained on a TRL-calibrated test vehicle with significant roughness on conductors made of three types of copper foils: a standard (STD)-roughness, very-low-profile (VLP), and hyper-very-low-profile (HVLP) foils.

Abstract: The transfer function of supply voltage fluctuation to jitter is analytically derived in closed form expressions for a single-ended buffer. The analytic transfer function is derived from the linear differential equation obtained
from asymptotic linear inverter I-V curves. The transfer functions are validated by comparison with HSpice simulations, and the estimated jitter is compared to simulated jitter in eye diagram with single-frequency and multi-tone supply noise.


**Abstract:** A fast method to calculate the admittance matrix of Through Silicon Vias (TSVs) is proposed in this talk. The silicon dioxide layers are equivalently modeled using the bound charge on the conductor surfaces as well as on the dielectric interface between the silicon dioxide and the silicon regions. Unknown surface densities of both the free and bound charge are expanded using the axial harmonics. Galerkin’s method is then applied to obtain the capacitance and conductance matrices. The proposed method is validated with a full-wave 2D cross-sectional analysis tool for a typical TSV pair structure. Comparisons with popular closed-form expressions are also discussed.

[Presentation 10]  “EMI Analysis of DVI Link Connectors,” by Soumya De, Yaojiang Zhang, Abhishek Patnaik, David Pommerenke, Chen Wang, Charles Jackson

**Abstract:** In the Digital Visual Interface (DVI) the DVI connector is an important link. The discontinuities in the connector itself can convert differential signals to common mode which can further produce antenna mode currents causing EMI. The overall goal of the study is to analyze the DVI connector by quantifying the effects of the discontinuities in the connector and the return path of the currents. This is done in a step-by-step manner by first analyzing the port voltages along the discontinuities in the connector and then measuring the radiated field for EMI analysis. In this presentation, we will discuss the measurement strategies and the results.

[Presentation 11]  “Capacitance Calculation of TSVs Using an Integral Equation Method Based on Partial Capacitances,” by Hanfeng Wang, Al Ruehli, and Jun Fan

**Abstract:** An integral equation method based on partial capacitances is used to extract the capacitance between two through-silicon-vias (TSVs). The unrealistic assumption of equal potential along the vertical interface of silicon dioxide (SiO2) coating of TSVs in the analytical method has been removed by introducing unknown equivalent charge. The Galerkin’s method is used here to solve the unknown charge densities in the integral equation and thus, the capacitance between two TSVs can be efficiently calculated. The results are validated by comparing the extracted capacitances with commercial software based on the finite element method. The accuracy and efficiency have been demonstrated.


**Abstract:** Vias sharing a common-antipad is a typical PCB geometry. Effective models for this geometry can provide accurate estimation of signal propagation
properties of via structures. In this talk, a fast hybrid finite element method is proposed. The method is validated using a few examples.

[Presentation 13] “System Efficient ESD Design (SEED),” by Tianqi Li, David Pommerenke
Abstract: An LED circuit of a cell phone is analysed using the System-Efficient-ESD-Design (SEED) methodology [1]. The method may clarify and reveal the ESD current path, and interaction mechanism between the clamp and on-chip ESD protection circuit of a given system. I-V curves and non-linear behavior obtained using high voltage pulses of every non linear component such as L, C, ferrite beads and IC pins are measured and modeled in addition to the linear parts, such as traces. By combining all of the component models together, a complete circuit model could be built for predicting the circuit behavior and damaging threshold under ESD contact-mode discharge or Transmission Line Pulser (TLP) injection by running SPICE simulation.

[Presentation 14] “Location of ESD Events in a Manufacturing Environment,” by Pratik Maheshwari, David Pommerenke
Abstract: The project uses a reverse time of arrival approach to perform localization of ESD events in a 3D space. The system uses 4 receiver antennas and captures the EM pulse generated from the ESD events. The time difference of arrivals between the received signals along with the locations of the antenna is used to locate the ESD event location in a 3D space. Other information like the ESD source strength, the energy of the source pulse and the type of ESD can also be estimated. The intended application is to detect ESD events and source locations in IC and PCB manufacturing locations.

[Presentation 15] “Investigation of the ESD Coupling into USB Port System,” by Fayu wan, David Pommerenke
Abstract: ESD to USB Connectors often hit the shell which is usually not well connected to a partial chassis. These simulations analyze basic coupling effects and parametric influence of different grounding configurations on voltages coupled to traces and to flex cable alike board to board connections.

Abstract: We present a new method for modeling both low frequency (10 KHz) and high frequency (~50 MHz) operation and EMC relevant coupling of transformers in SPICE. The resulting model is based on a two dimensional cross sectional numerical model of a device geometry which can be implemented in SPICE simulations. Using this improved transformer model, distributed capacitive parasitics can be accurately included in early SPICE simulations to reveal the high frequency behavior of the transformer, in particular the common mode leakage currents across isolated windings.
**Presentation 17**  
“Cable Attachment to Huygen’s Surfaces,” by Keong Kam, David Pommerenke  
**Abstract:** Near-field scanning is often used to solve EMC problems. Aside from the purpose of visualization of near-fields, measured near-field data can be used to estimate far-field. One of many challenges associated with using near-field to far-field transform (NFFFT) technique for EMC application is the handling of attached cables. The objective of this investigation is to evaluate different methods to add cable information to the near-field data for far-field estimation comparing corresponding assumptions, accuracy, and practicality. The investigation is carried out first using numerical experiments in EMcos EMC studio, which is a commercial MoM (Method of Moment) tool for EM simulation. Measurement results from real test structure are also presented to validate the results from numerical experiments.

**Presentation 18**  
“Methods for Reducing Emissions from Switching Power Circuits,” by Todd Hubing  
**Abstract:** This presentation describes two methods for reducing radiated emissions from power circuits such as DC-to-DC converters and 3-phase motor drivers. The first method involves the insertion of a passive pi-filter on the output. (All three phase outputs in the case of the motor driver.) The pi-filter utilize the parasitic inductance of the output trace and works very well at frequencies from about 10 MHz to 100 MHz. The second method is an active noise cancellation device that works well at lower frequencies. It is expected that the active cancellation device will eventually be an effective approach up to frequencies as high as 10 MHz. These two methods together will significantly reduce unwanted common-mode currents due to power inverters over the entire frequency range of interest.

**Presentation 19**  
“Predicting System-Level Radiated Emissions from Component-Level Measurements of a Power Inverter,” by Todd Hubing  
**Abstract:** As part of an earlier EMC center project, a method for measuring circuits in a TEM-cell and utilizing the results to model these circuits in full-wave simulations was developed and validated. This presentation describes the application of this technique to a power inverter circuit. There is excellent agreement between model results and radiated emission measurements of the power inverter with attached cables of arbitrary length and orientation.

**Presentation 20**  
“Methods for channel block de-embedding using recursive convolution, (frequency domain) and FIR filtering approaches” by Alexander Razmadze, Arun Reddy Chada, Jun Fan, James L. Drewniak  
**Abstract:** As data rates continue to increase, losses in transmission channels and fixtures can impact the accuracy of an eye diagram measurement dramatically. De-embedding of fixture and channel effects from measured data must be employed in order to reconstruct the true signal at the DUT from the measured waveform on the far end of the transmission channel. In this talk de-embedding
approaches using recursive convolution, (frequency-domain) approach and FIR filter-based approaches are discussed and compared.

[Presentation 21] “Errors in $\varepsilon'$ (DK) and $\tan\delta$ (DF) Extraction for PCB Material Using a Traveling Wave Measurement Method,” by Aleksandr Gafarov, James Drewniak

**Abstract:** The necessity of getting accurate $\varepsilon'$ (DK) and $\tan\delta$ (DF) on low-loss Printed Circuit Boards (PCB) over a frequency range of 0.50GHz – 50GHz is a important requirement for high-data-rate design. One method for characterizing material is a traveling wave measurement method. It is necessary to have a good TRL calibration up to 50 GHz for deembedding via and connector transitions. There are problems in the method that can cause errors and uncertainties. Challenges include non-ideal uniformity of connector mounting and transitions, surface roughness o losses in DF, deviation of the characteristic impedance from 50 $\Omega$ of the traces, incorrect TRL patterns that is a result from using a common calibration pattern set over wide Dk, non-uniformity of DUT and TRL patterns, mismatch of the pad sizes of the via and connector, non-ideal structure of via stubs, imperfect design of the via wall connecting the stripline reference planes, non-symmetrical position of the DUT regarding to ground planes, manufacturing errors, instrument systematic error.

[Presentation 22] “Switching-Current Measurement for Multiple ICs Sharing a Common Power Island Structure,” by Tao Wang and Jun Fan

**Abstract:** Abstract: Switching currents in active integrated circuits (ICs) generate noise in the power distribution network (PDN), which is one of the main sources for many signal/power integrity and electromagnetic interference issues in high-speed electronic devices. Accurate knowledge of the switching currents is the key to ensure a good PDN design. This talk proposes a measurement methodology, when IC information is not available, to obtain the equivalent switching current of each IC in the case where multiple ICs are connected to a common power island structure. Time-domain oscilloscope measurements are used to capture the noise-voltage waveforms at a few locations in the power island. Combining with the multi-port frequency-domain S-parameter measurement among the same locations, an equivalent switching current for each IC is calculated. The proposed method is validated at a different location in the power island by comparing the calculated noise voltage using the equivalent switching currents as excitations with the actual measured noise voltage.

[Presentation 23] “Over the air test for wireless terminals – Technical challenges and solutions,” by Yihong Qi

**Abstract:**

Abstract: Sensitivity analysis of the performance of thin absorbing coatings and ferrite chokes on cables to the variation in dielectric and magnetic properties of materials is carried out. This variation corresponds to possible uncertainty in measuring complex permittivity and permeability of materials. The analysis in this paper is done numerically using the 2D-FEM code. The modeled parameters are input impedance and EMI radiation reduction when applying absorbing materials and ferrite chokes on the cables, represented as monopole antenna rods. The material parameters of absorbing materials and ferrites used in this study were measured using the standard 7/3-mm coaxial air line. Higher sensitivity of the modeled parameters to the uncertainty of measuring complex permeability of absorbing materials and ferrites, and lower to the uncertainty of measuring complex permittivity, even in the case of high-permittivity absorbing coatings, have been demonstrated.

Abstract: Dielectric properties are important for accurate and effective signal and power integrity simulations. In this presentation, plane-pair geometries are used to extract the dielectric properties in a wide frequency range based on a proven via-plane model and optimization.

[Presentation 26] “A Test IC for Developing Models of IC Immunity,” by Xu Gao, David Pommerenke
Abstract: Integrated circuits (ICs) are often responsible for failures in electrical systems, but few system-level models exist to predict when or why these failures will occur. In order to investigate the failure mechanism of ICs due to external noise and to develop analytic sub-models to predict when the ICs will fail, a test IC was designed and fabricated. Four basic circuit structures common to most digital ICs are included in this test IC, including an inverter chain (logic block), delay lock loop, SRAM unit, and a crystal oscillator. An explanation of the IC design and testing approach and of preliminary simulation results will be given.

[Presentation 27] “Measurement-Based Model for IC Immunity,” by Victor Khilkevich, David Pommerenke
Abstract: The immunity of the integrated circuits (IC) is one of the major topic of EMC. If the geometry of the package and the circuit diagram of the IC is available, a model describing IC immunity can be built relatively easily. However, on practice, such information is rarely available to EMC engineers, and the model has to be built based on the limited knowledge of the IC internal structure. The methodology of developing an IC immunity model based on the measurements is presented in this paper, which has three parts: 1) definition of the IC failure criteria; 2) experimental characterization of the IC in terms of the selected criteria; and 3) development of the models reflecting the measured characteristics. Future work will be devoted to the experimental validation of the models.
Abstract: Link path analysis using Fast EM Analysis Suite (FEMAS) is presented in this talk. The fully functional features are currently 2D cross-sectional analysis tool, advanced plotting capabilities, causality and passivity checking/enforcement tools and material library with functionality to fit tabulated material characteristics by N-term Debye models. Under QA assessment and in the polishing stage it has FD/TD link path analysis modeling with delay extraction, pre-emphasis, and generating S-parameters from circuit blocks imported from SPICE files. Upcoming features are jitter decomposition, stressed jitter analysis, and equalization.

Abstract: A physics-based circuit model has been developed for fast simulation of printed circuit board (PCB) power distribution network (PDN) structures, based on the cavity method. The physics-based nature of the model completes our “Geometry – Model – Response” design paradigm, enabling a study of design discovery scenarios. Design guidelines are developed for a high layer count stack up and many decoupling capacitors connected to an IC footprint on the PCB. These guidelines help understand the trends and tradeoffs in PDN design decisions in high layer count PCBs, while using the PDN impedance as a metric for design.

[Presentation 30] “Identification and Visualization of the electromagnetic Coupling Path,” by Hongyu Li
Abstract: This research investigates methods to identify and visualize electromagnetic coupling paths. Four frequency-domain methods were introduced on a previous meeting. Frequency-domain methods are based on time-averaged steady-state sinusoidal signals. In order to solve arbitrary time dependent problem effort was made to develop a more general time-domain method. This talk will update on the research results mainly for the time-domain method and show applications.